**Amendments to the Claims:**

This listing of claims will replace all prior versions, and listings of claims in the application:

**Listing of Claims:**

1. (Previously Presented) An alternating current signal level detection circuit comprising:

a first comparator (52, 82) which receives a rectified voltage obtained by rectifying an alternating current signal generated by an alternating current power source, compares an instantaneous value of the rectified voltage with a first reference voltage (V2), and represents by a first comparison result periods in which the instantaneous value exceeds the first reference voltage;

a second comparator (40, 70, 90) which compares the instantaneous value of the rectified voltage with a second reference voltage (V1) which is higher than the first reference voltage, and represents by a second comparison result periods in which the instantaneous value exceeds the second reference voltage;

a storage unit (53a, 54, 83a, 84) which stores information representing whether or not the rectified voltage exceeds the second reference voltage in each period in which the instantaneous value exceeds the first reference voltage (V2), based on the first comparison result and the second comparison result; and

a determination signal output unit (53b, 55, 83b, 85, 86) which represents by a high-low determination signal whether a level of the alternating current signal generated by said alternating current power source is high or low in each cycle of the rectified voltage, based on the information stored in said storage unit.

2. (Previously Presented) The alternating current signal level detection circuit according to claim 1, wherein said determination signal output unit represents by the high-low determination signal that the level of the alternating current signal generated by said alternating current power source is high when said storage unit stores information representing

that the rectified voltage exceeds the second reference voltage, and represents by the high-low determination signal that the level of the alternating current signal generated by said alternating current power source is low when said storage unit stores information representing that the rectified voltage does not exceed the second reference voltage.

3. (Previously Presented) The alternating current signal level detection circuit according to claim 1, wherein the rectified voltage is a voltage obtained by full-wave-rectifying the alternating current signal.

4. (Previously Presented) The alternating current signal level detection circuit according to claim 2, wherein said determination signal output unit (53b, 55) represents by the high-low determination signal whether the level of the alternating current signal is high or low by referring to the information stored in said storage unit (53a, 54) when a level of the rectified voltage passes over the first reference voltage (V2) from a higher side to a lower side.

5. (Withdrawn) The alternating current signal level detection circuit according to claim 2, wherein said determination signal output unit (83b, 85, 86) represents by the high-low determination signal whether the level of the alternating current signal is high or low by referring to the information stored in said storage unit (83a, 84) when a level of the rectified voltage exceeds the second reference voltage (V1) and when the level of the rectified voltage passes over the first reference voltage (V2) from a higher side to a lower side.

6. (Previously Presented) The alternating current signal level detection circuit according to claim 4, wherein

said storage unit comprises:

a reset signal output unit (53a) which generates and outputs a reset signal (P1) based on the first comparison result of said first comparator (52) when the instantaneous value of the rectified voltage passes over the first reference voltage (V2) from the lower side to the higher side; and

a reset-set flip-flop circuit (54) which outputs a Q signal which is reset based on the reset pulse (P1) generated by said reset signal output unit (53a) and which is set based on the second comparison result of said second comparator (42) representing that the instantaneous value of the rectified voltage exceeds the second reference voltage (V1), and stores a reset or set status of the Q signal, and

said determination signal output unit comprises:

a timing signal output unit (53b) which generates and outputs a timing signal (P2) based on the first comparison result of said first comparator (52) when the instantaneous value of the rectified voltage passes over the first reference voltage (V2) from the higher side to the lower side; and

a delay flip-flop circuit (55) which refers to the reset or set status of the Q signal output from said reset-set flip-flop circuit (54) when the timing signal (P2) is output from said timing signal output unit (53b), and outputs a signal having a same status as the status referred to as the high-low determination signal.

7. (Withdrawn) The alternating current signal level detection circuit according to claim 5, wherein

said storage unit comprises:

a reset signal output unit (83a) which generates and outputs a reset signal (P1) based on the first comparison result of said first comparator (82) representing that the instantaneous value of the rectified voltage exceeds the first reference voltage (V2); and

a reset-set flip-flop circuit (84) which outputs a Q signal which is reset based on the reset signal (P1) generated by said reset signal generation unit (83a) and which is set based on the second comparison result of said second comparator (72) representing that the instantaneous value of the rectified voltage exceeds the second reference voltage (V1), and stores a reset or set status of the Q signal as the information, and

said determination signal output unit comprises:

a timing signal output unit (83b) which generates and outputs a timing signal (P2) based on the first comparison result obtained by determination of said first comparator (82);

a delay flip-flop circuit (85) which refers to the reset or set status of the Q signal output from said reset-set flip-flop circuit (84) when the timing signal (P2) is output from said timing signal output unit (83b), and outputs a signal having a same status as the status referred to; and

a logical OR operation unit (86) which implements a logical OR operation of an output signal from said reset-set flip-flop circuit (84) and said delay flip-flop circuit (85), and outputs a result of the logical OR operation as the high-low determination signal.

8. (Previously Presented) The alternating current signal level detection circuit according to claim 2, comprising a first power source having the first reference voltage (V2) and a second power source having the second reference voltage (V1), wherein:

said first power source lowers the first reference voltage (V2) when the instantaneous value of the rectified voltage passes over the first reference voltage (V2) from a lower side to a higher side; and

said second power source lowers the second reference voltage when the instantaneous value of the rectified voltage passes over the second reference voltage from a lower side to a higher side.

9. (Previously Presented) An alternating current signal level detection circuit comprising:

a first comparator (52) which receives a rectified voltage obtained by rectifying an alternating current signal generated by an alternating current power source, compares an instantaneous value of the rectified voltage with a first reference voltage (V2), and represents by a first comparison result periods in which the instantaneous value exceeds the first reference voltage;

a second comparator (43) which compares the instantaneous value of the rectified voltage with a plurality of second reference voltages (V1, V3) which are higher than the first

reference voltage, and represents by a second comparison result periods in which the instantaneous value exceeds any one of the second reference voltages;

a storage unit (53a, 54) which stores information representing whether or not the rectified voltage exceeds the second reference voltages in each period in which the instantaneous value exceeds the first reference voltage (V2), based on the first comparison result and the second comparison result; and

a determination signal output unit (53b, 55) which represents by a high-low determination signal whether a level of the alternating current signal generated by said alternating current power source is high or low in each cycle of the rectified voltage, based on the information stored in said storage unit.

10. (Previously Presented) The alternating current signal level detection circuit according to claim 9, comprising a first power source having the first reference voltage (V2) and a second power source having the second reference voltages (V1, V3), wherein:

said first power source lowers the first reference voltage (V2) when the instantaneous value of the rectified voltage passes over the first reference voltage (V2) from a lower side to a higher side; and

said second power source lowers the second reference voltages when the instantaneous value of the rectified voltage passes over the second reference voltages from a lower side to a higher side.